

# The Silicon Pixel Tracker – beginning of a revolution?

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The SPT concept was first presented by Konstantin Stefanov in March 2008. Shortly afterwards, STFC ‘ceased investment’ in ILC, but internationally, interest in the SPT has grown steadily, not only for the linear collider.

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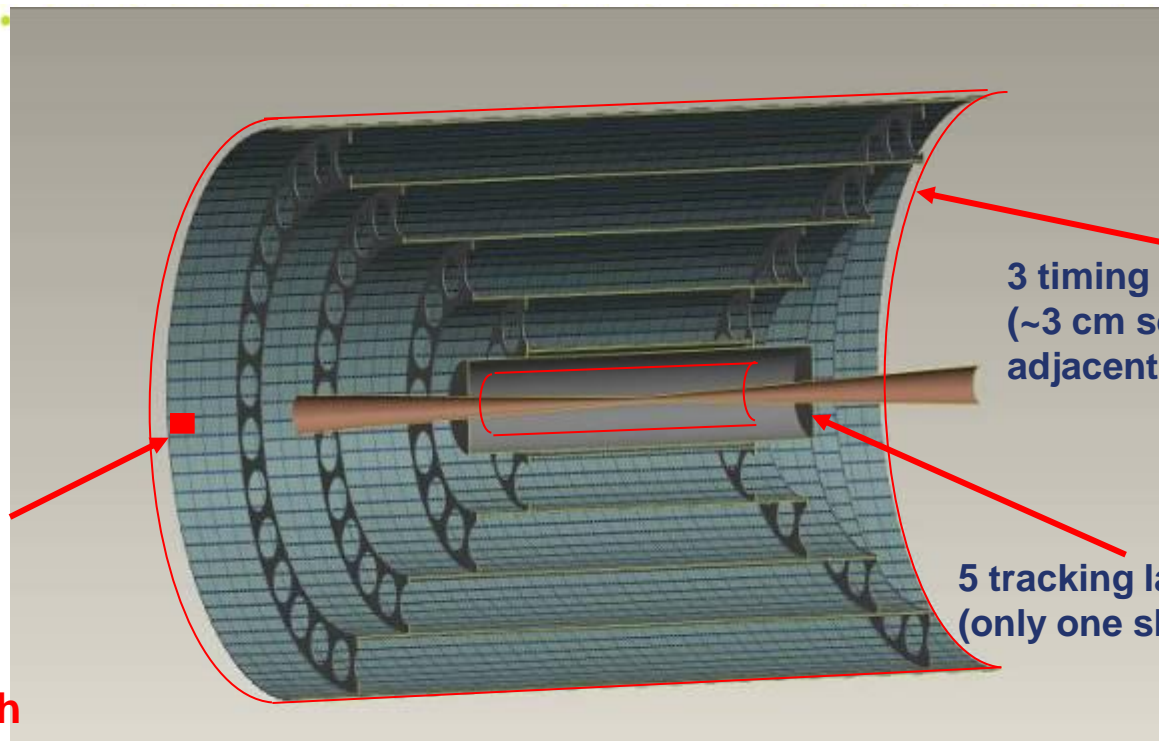
- **Design concept**
- **Mechanical simulations**
- **Feasibility** – new results with advanced CMOS pixels from:
  - Jim Janesick (California) working with Jazz Semiconductors and
  - Dave Burt et al (e2V and Open U) working with Tower Semiconductors} *foundries*  
} *now united*
- Next steps - **performance simulations**
- Practical realization for LC and other applications (possibly including LHC)

## Design Concept – LC as one real-life example (1)

- **Basic goal is to devise a tracker design which significantly reduces the material budget wrt the currently projected leader, the SiD silicon microstrip tracker, which uses the same technology as the LHC GPD trackers**
- **Why push to minimise material in tracker?**
- **In general, we would like photons to convert in the ECAL not in the tracking system**
- **Looking at previous tracking systems, they have all ‘gone to hell in the forward region’**
- **This has diminished the physics output. Since we don’t have any counter-examples, it’s difficult to quantify**
- **At higher energies, most events have jets in the forward region. ‘A chain is as strong as its weakest link’**
- **Examples for LC physics: Reconstruction of  $\pi^0$ s in jets could significantly improve B/charm separation (a very general tool)**
- **A more transparent tracker may deliver a significant advantage in ‘luminosity factor’. Given the cost of *operating* the accelerator system, a somewhat more expensive tracking system may be highly cost-effective**

## Design Concept – LC as one real-life example (2)

- The largest pixel tracking system in HEP (the SLD vertex detector with 307 Mpixels) used CCDs. Advanced CMOS pixels have evolved from this technology, achieving far higher functionality by in-pixel and chip-edge signal processing
- **Basic SPT concept is a ‘separated function’ design – precision timing on every track *but not on every point on the track*. So we suggest an optimised mix of tracking layers and timing layers.**
- Key features are binary readout and on-sensor data sparsification. Also, timing layers with appropriate precision (~10 ns for CLIC; 300 ns for ILC)
- Thin monolithic ***charge-coupled CMOS pixels*** offer a different ‘separated function’ feature – evading the link between charge collection and charge sensing, with great advantages as regards power dissipation and noise performance
- By working with a *monolithic planar architecture* (CMOS technology) the systems will be scalable by 2020 to the level of ~40 Gpixels
- This design has evolved within the international SiLC collaboration, since UK support was withdrawn 3 years ago



**Tracking sensor, one of 12,000, 8x8 cm<sup>2</sup>, 2.56 Mpixels each**

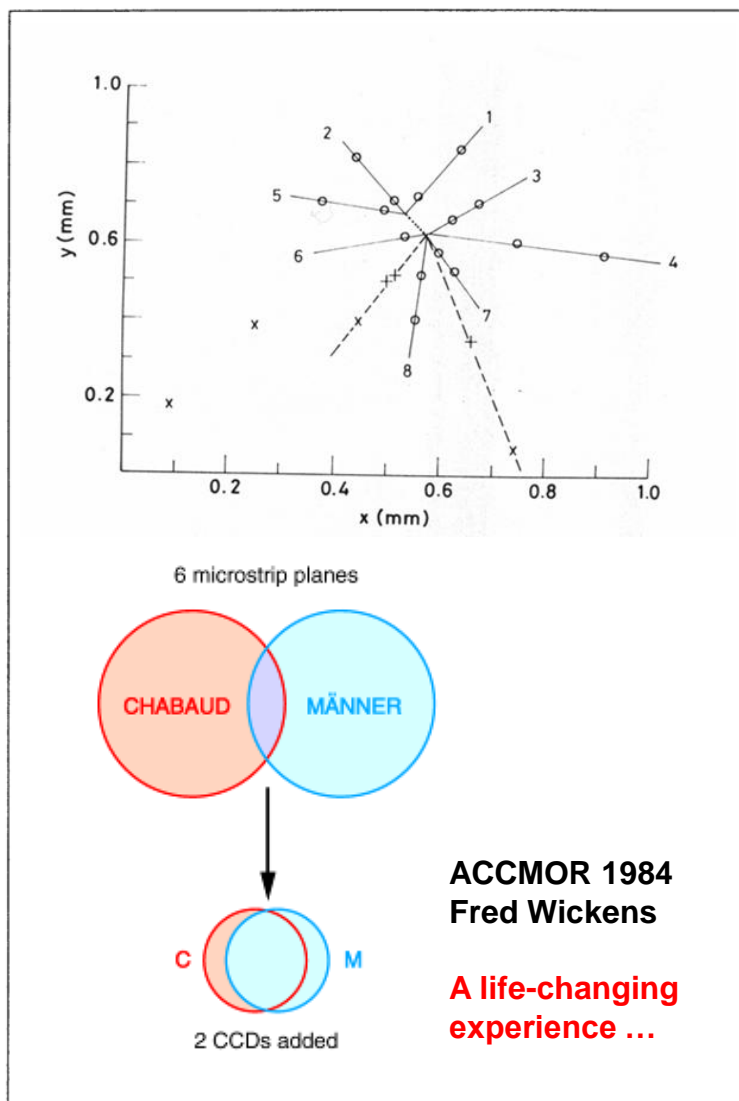
**3 timing layers with endcaps (~3 cm separation between adjacent layers)**

**5 tracking layers with endcaps (only one shown)**

- Derived from SiD 5-layer microstrip tracker
- **Barrels:** SiC foam ladders, linked mechanically to one another along their length
  - **Tracking layers:** 5 cylinders,  $\sim 0.6\% X_0$  per layer,  $3.0\% X_0$  total, over full polar angle range  $\sim 50 \mu\text{m}$  square pixels
  - **Timing layers:** 3 cylinders as an envelope,  $\sim 1.5\% X_0$  per layer if evaporative  $\text{CO}_2$  cooling, but may also be amenable to gas cooling ( $\sim 1.3$  kW overall)  $\sim 150 \mu\text{m}$  square pixels
- **Matching endcap layers:** 5 tracking and 3 timing (envelope)

# Track reconstruction

- Start with **mini-vectors** from on-time tracks found in the triplet of timing layers, together with an approximate IP constraint. Check for consistency with ECAL
- Work inwards through each successive tracking layer, refining the track parameters as points are added
- K-shorts, lambdas and photon conversions will be findable, starting from the mini-vectors in the timing layers, omitting the IP constraint and substituting a  $V^0$  constraint
- Background level (~7000 out-of-time tracks at CLIC at 3 TeV) appears daunting at first sight, but pixel systems can absorb a very high density of background without loss of performance
- General principle, established in vertex detectors in ACCMOR (1980s) and SLD (1990s): **fine granularity can to a great extent compensate for coarse timing. Precision time stamping costs power, hence layer thickness, fine granularity need not**
- Back-of-envelope calculations look promising (LCWS Warsaw 2008); looking forward to real simulations in near future
- Flexible design - if required by simulations, could make background rejection more robust, for example by switching one or more endcap tracking layers to timing

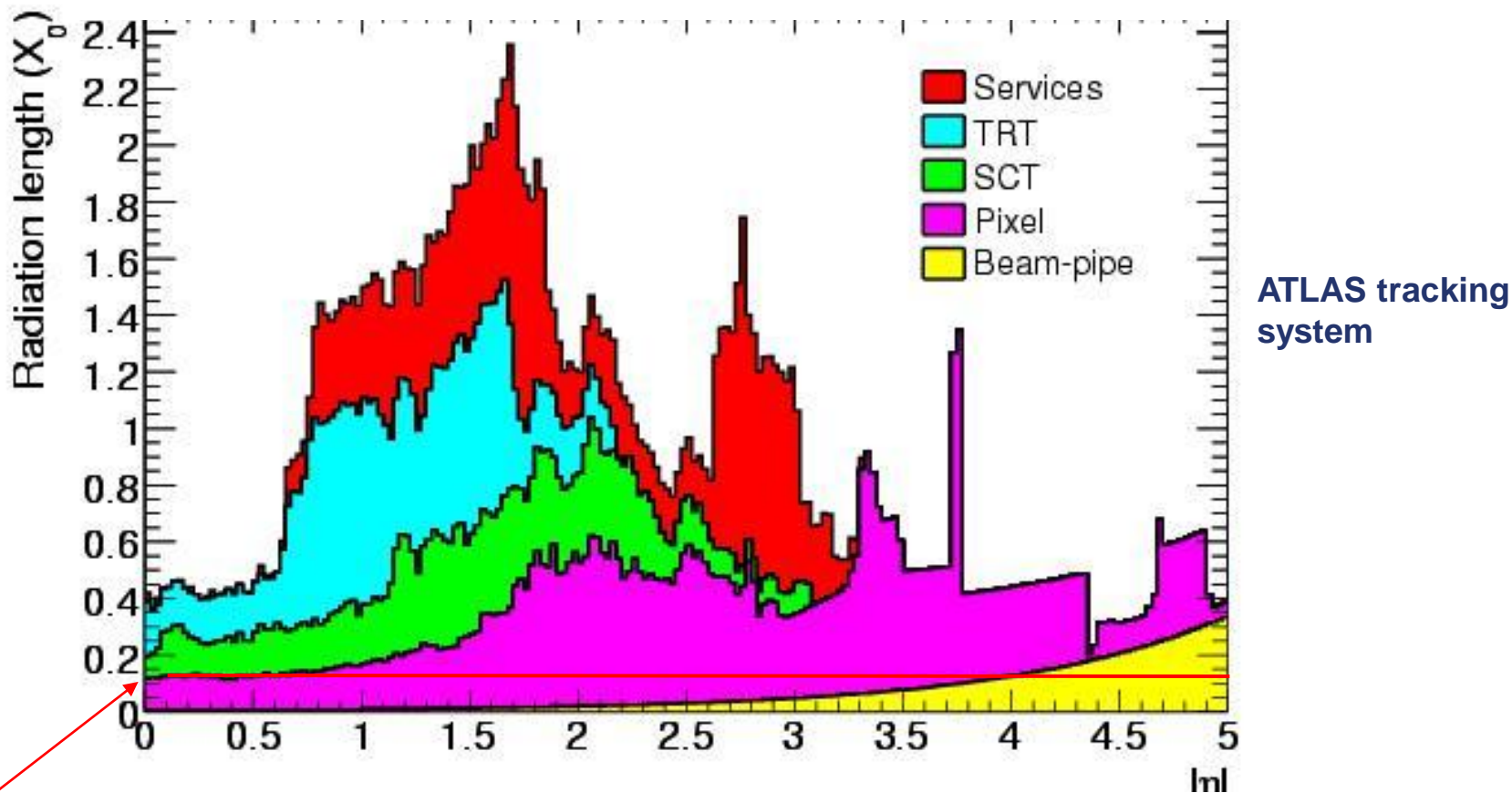


- 5 layers of microstrips may be marginal
  - For  $V^0$ s, microstrips need help for track reconstruction from the ECAL
- On the contrary, 5 tracking pixel layers may be overkill
- Track reconstruction in ATLAS and CMS of Pb-Pb collisions is a good demonstration of power of pixel systems
- C Rubbia at CERN 50<sup>th</sup> Nobel talks:
  - “Reason for lack of success at the ISR – **where most discoveries were missed** – was due to the poor quality of the detectors”
  - Also, remember the 40 GeV top signal in UA1 in 1984, due to lack of a vertex detector

- **Mechanical design** – can such large and lightweight structures be made sufficiently stable?
- **Overall scale** - 33 Gpixels for tracking layers, 5 Gpixels for timing layers. Reasonable, given progress in astronomy etc
- Need excellent **charge collection efficiency**, non-trivial for these relatively large pixels. Allowed to be slow for tracking layers but needs to be fast for timing layers (<10 ns for CLIC, ~100 ns for ILC), hence fully depleted structures to 30  $\mu\text{m}$  depth
- Need **good noise performance**, due to small signals from thin layers. Achievable, due to recent advances in charge-coupled CMOS pixels – **a fast-moving technology**
- Let's consider these issues in turn ...



# Material budget - a major challenge



10%  $X_0$ , a frequently-suggested goal for the LC tracking systems (recently abandoned by LCTPC collab, but still the goal for SiD)

Our goal is <1% (VXD) plus ~3% (main tracker) ie ~4% total, followed by outer timing layers which may add ~2% [plus the inevitable obliquity factors]





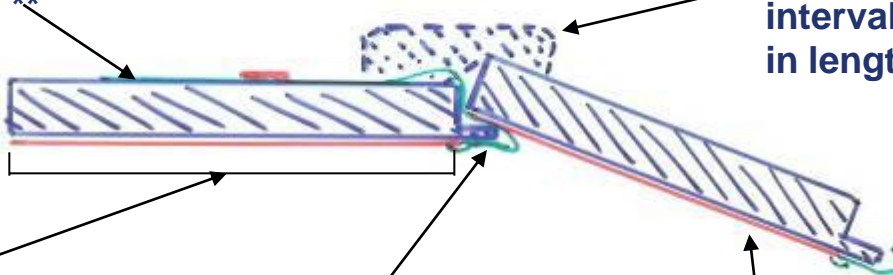
## End view of two barrel ladders ('spiral' geometry)

**Adhesive-bonded *non-demountable* structure is 'daring' but justified by experience with gas-cooled systems (SLD, astronomy)**

SiC foam, ~5% of solid density

\*\*

wedge links at ~40 cm intervals, each ~1 cm in length



Sensor active width 8 cm, with ~2 mm overlaps in  $r\phi$

thin Cu/kapton tab (flexible for stress relief), wire bonds to sensor

devices will be 2-side buttable, so inactive regions in  $z$  will be ~ 200  $\mu\text{m}$  (0.2%)

Sensor thickness ~50  $\mu\text{m}$ , 30  $\mu\text{m}$  active epi layer

\*\* Single layer Cu/kapton stripline with one mesh groundplane runs length of ladder, double layer in region of tabs (~5 mm wide) which contact each sensor.

Similar stripline runs round the end of each barrel, servicing all ladders of that barrel.

Sparsified data transmitted out of detector on optical fibres (1 or 2 fibres per end), continuously between bunch trains

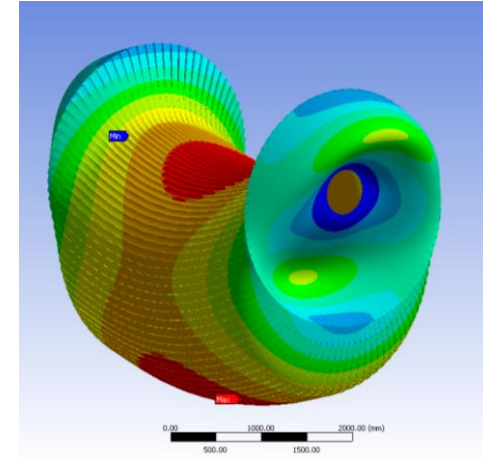
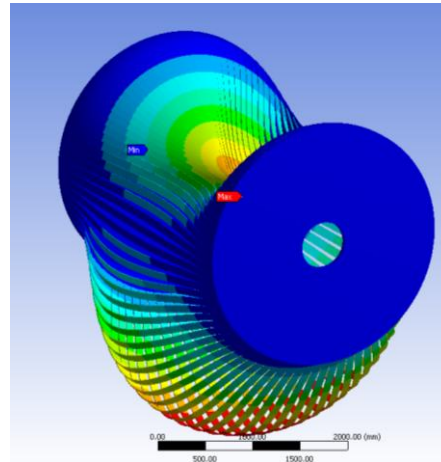
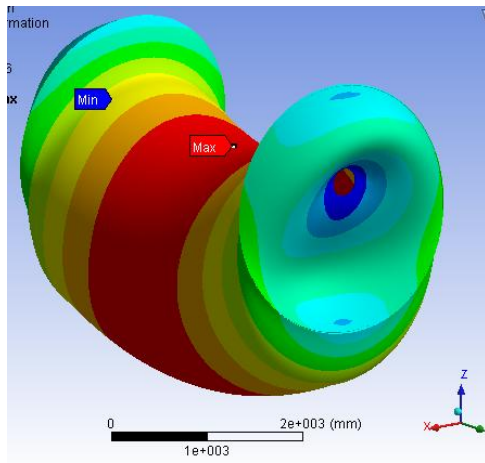
**Continuous (not pulsed) power for tracking layers, so minimal cross-section of power lines**

Tracking layers cooled by a gentle flow of nitrogen or air, hence no cooling pipes within tracking volume.

Timing layers need pulsed power, but current estimates suggest that gas cooling may suffice here also.

- SiC foam favoured wrt 'conventional' CFC sandwich, due to:
  - Homogeneous material, ultra-stable wrt temp fluctuations
  - Accurate match of expansion coefficient to Si, so bonding of large flexible thinned devices to substrate works well
- But what about the lower elastic modulus of SiC? A structure made of discrete ladders supported at ends would sag unacceptably under gravity
- Idea of non-demountable adhesive-bonded closed half-barrels was devised to minimise material budget (and is justified by long-term reliability of large pixel systems in space and other applications)
- This permits **small foam links** between ladders, both in the endcaps and in the barrels.
- Demonstrated that this spectacularly improves the shape stability, almost to the level of a continuous cylinder
- System is assembled as pairs of closed half-barrels, sequentially onto the beampipe after the vertex detector, starting with the innermost layer

# ANSYS simulation of Layer 5



- Continuous foam cylinder
- Max deflection **10  $\mu\text{m}$**

- Separate foam ladders
- Max deflection **20.5 mm**

- Ladders joined by small foam piece every 40 cm
- Max deflection **20  $\mu\text{m}$**

Steve Watson - RAL

## Growth of CCD mosaics

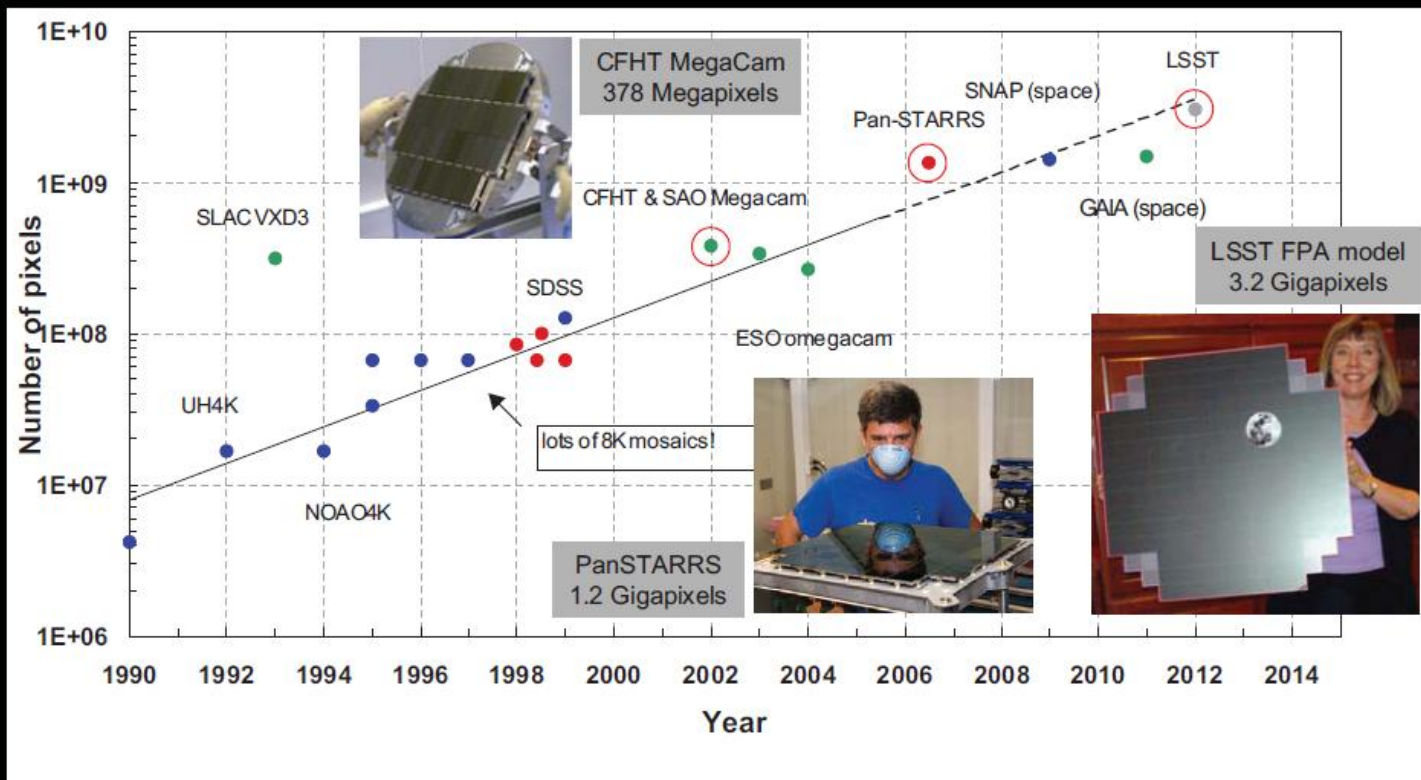


Illustration of large focal plane sizes, from Luppino 'Moore's' law

Focal plane size doubles every 2.5 years

LSST R&D going well – final stages of prototyping. 40 Gpixels will be 'on the line' by 2020.

Note also VXD3!

25 May 2011

Recent results from Jim Janesick, reported at workshop on imaging systems for astronomy, San Diego, June 2010. Figure from Janesick SPIE 7742-11 (2010)

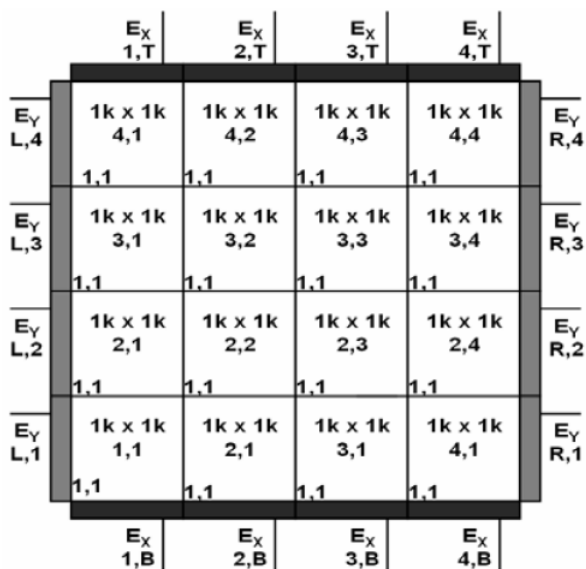


Figure 15. Block diagram of a stitched 4k x 4k imager.

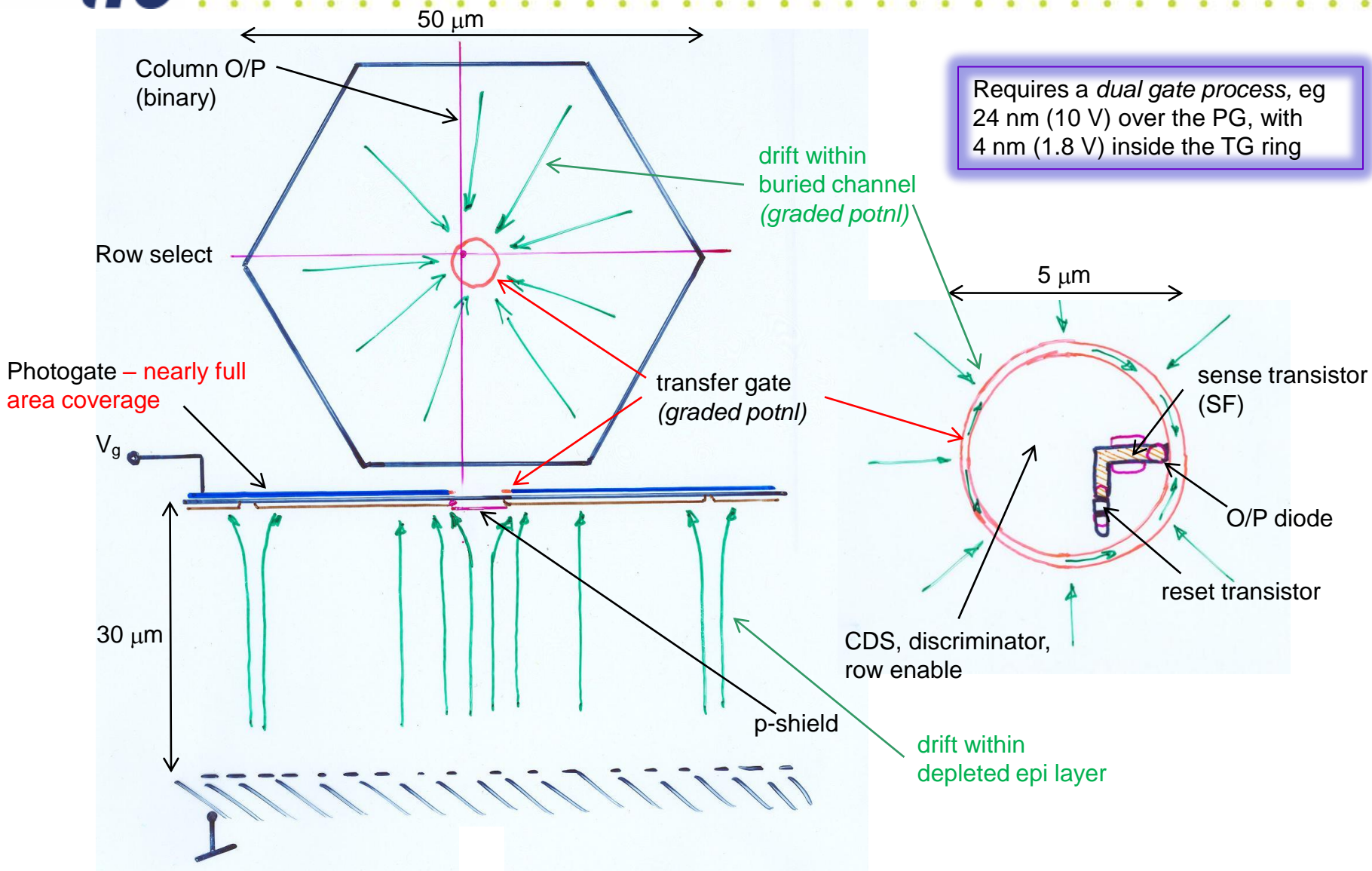
4 x 4 cm<sup>2</sup> devices in Sandbox 6 (SB 6). Yields are 'high'.  
10 x 10 cm<sup>2</sup> devices being processed this year in SB 7

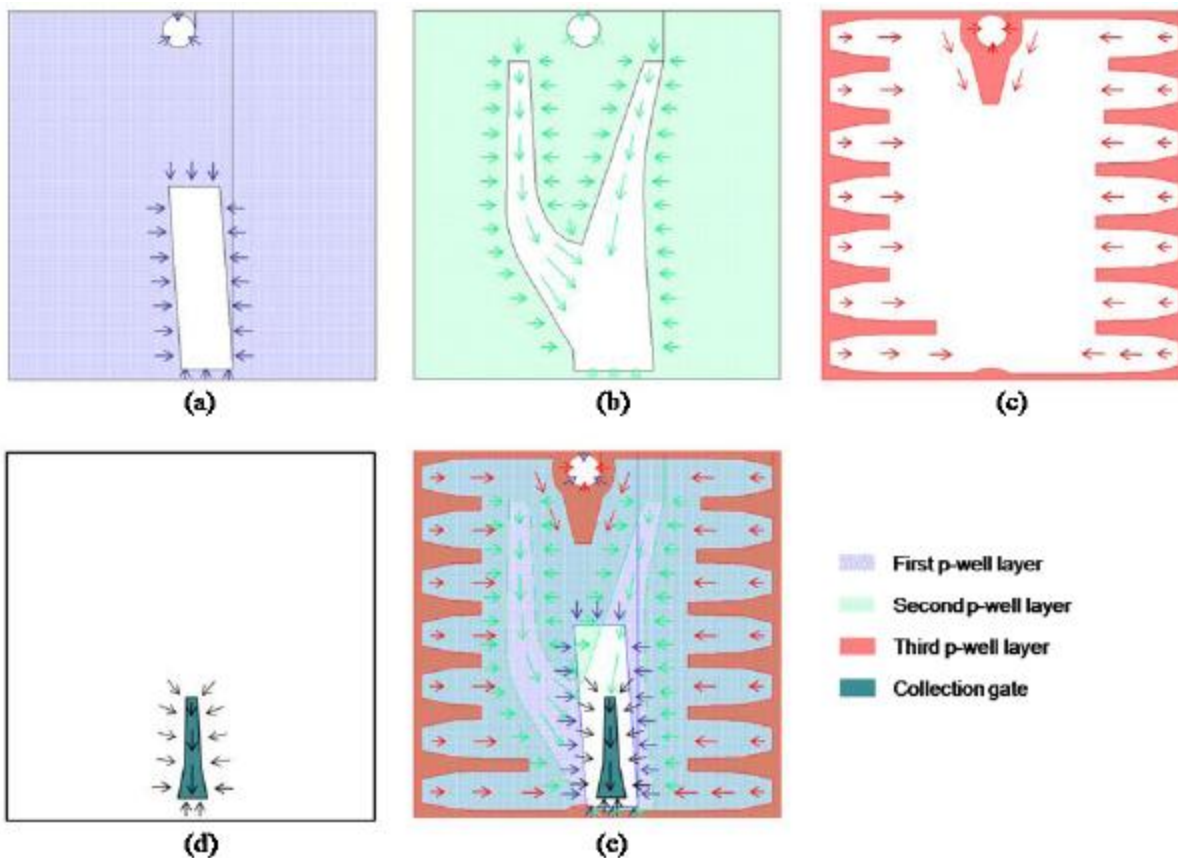


**World's largest CMOS imaging sensor,  
by Canon Inc, 20.2x20.5 cm<sup>2</sup>  
(thanks to Norm Graf for the link)**

# Tracking pixel – unit cell

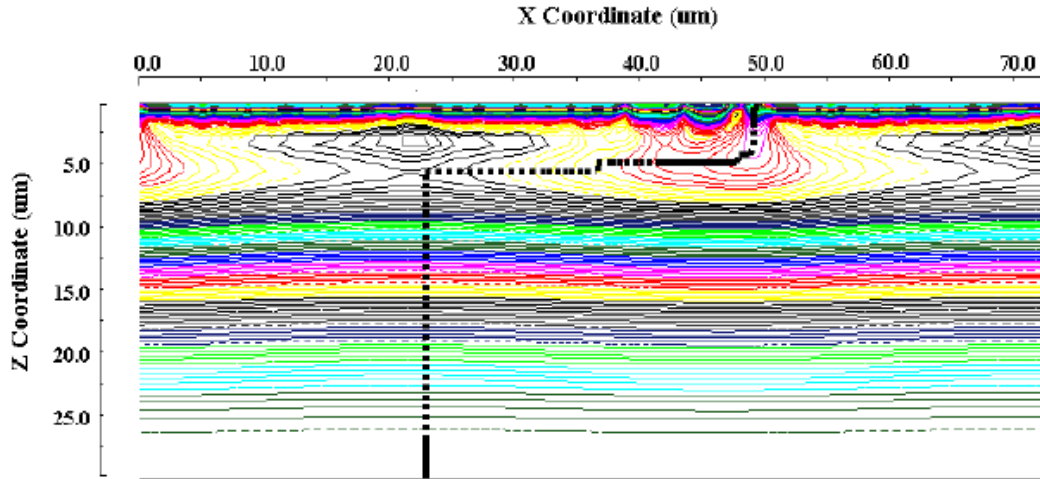
Requires a *dual gate process*, eg 24 nm (10 V) over the PG, with 4 nm (1.8 V) inside the TG ring





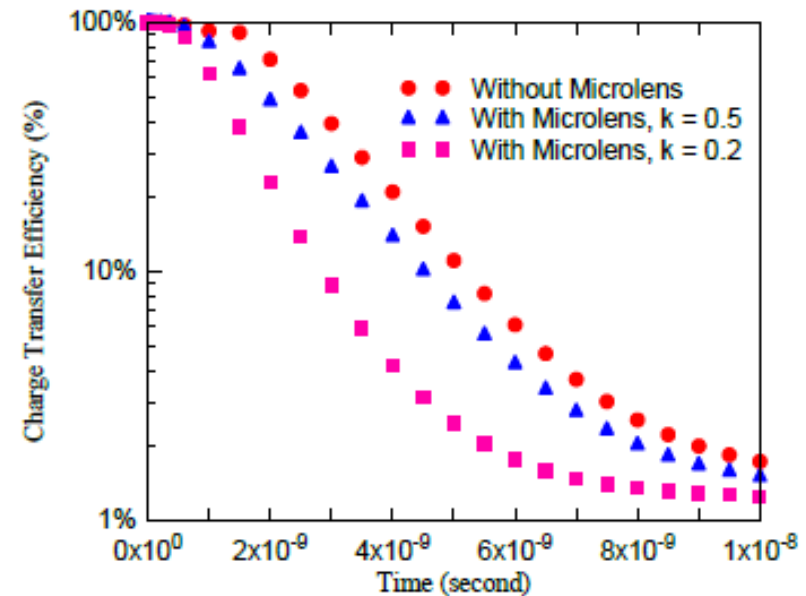
Relatively simple – all implants can be made at the same energy  
 Goji Etoh, 2009





90% charge collection within  
~5 ns from uniform  
illumination of back surface  
(simulation)

Goji Etoh, 2009



e2V has developed similar implant structures, starting with their supplementary channels 20 years ago. The 5 V/1.8 V dual gate process at Jazz may suffice, but higher voltage can be developed if needed. Other foundries (eg IBM) offer dual-gate processes for various high voltage applications – this trend is increasing for mixed analogue/digital devices [low tunneling currents needed for analogue; small device sizes needed for digital]



# Timing layers for ILC or CLIC

Regions where 'full' time stamping is needed – 300ns or 10 ns

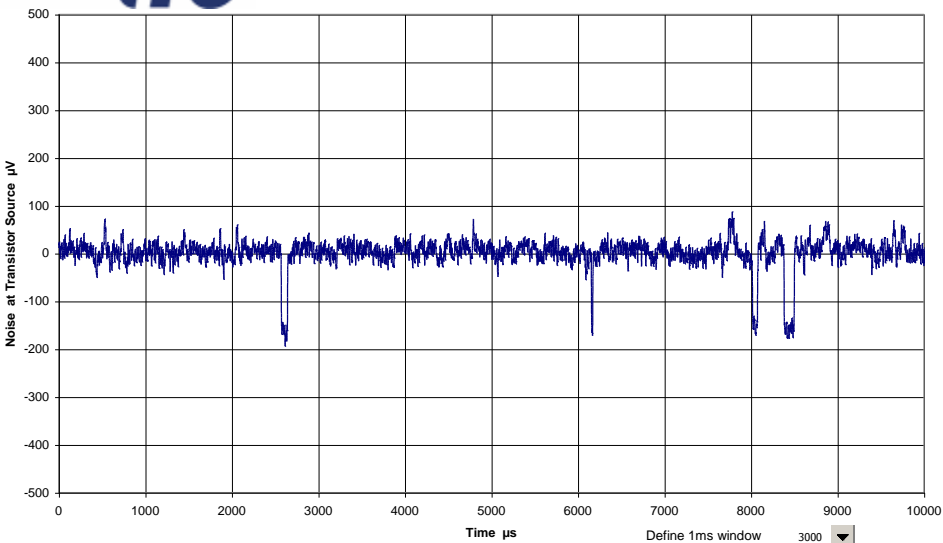
Timing pixels (~150  $\mu\text{m}$  diameter):

- Fast charge collection from larger pixels needs device simulation
- Front-end comprises in-pixel sense transistor, CDS and discriminator, as for tracking layers
- But now, CDS spans bunch train (1 ns or 180 ns): **Sample-1** before start of train, then open TG. **Sample-2** senses the true time of charge collection in pixel
- Add time stamp – send fast column signal to periphery, pick up bunch crossing number and store in edge memory
- Also send to periphery (more leisurely column signal) row address and store that
- Between bunch trains, read addresses and time information of hit pixels
- **Higher power dissipation of continuously active front-end increases power dissipation (from ~300 W to ~1.3 kW), but still reasonable for gas cooling**

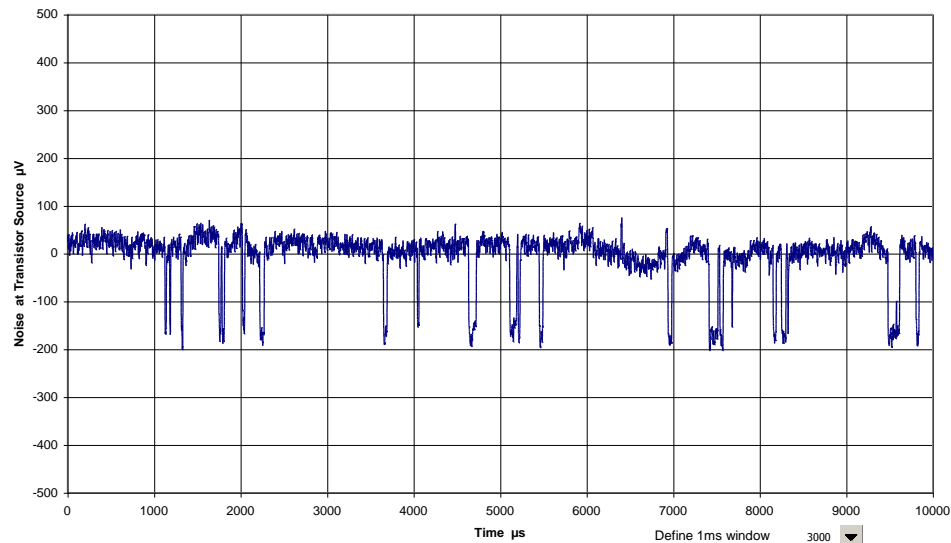


# RT Noise

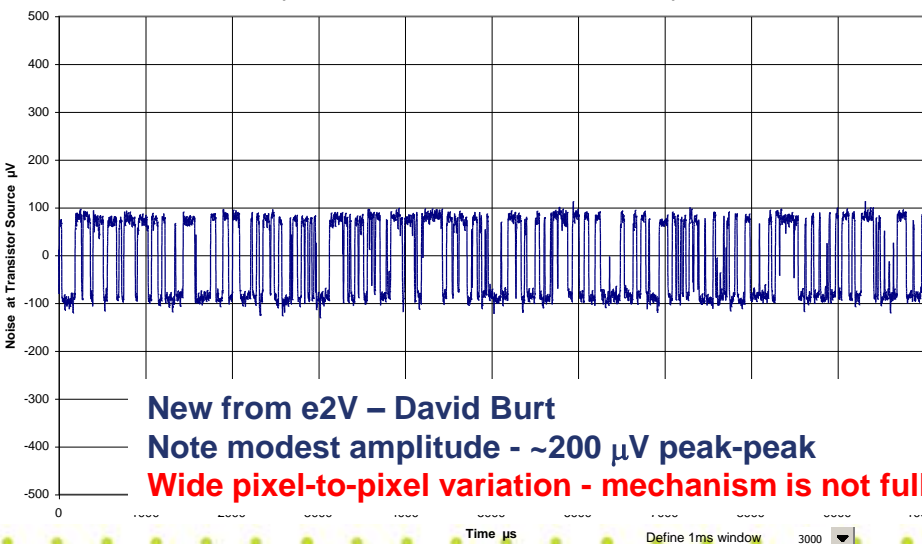
RTS noise plot of CMOS Test Transistor W1-5 at a current of 1 $\mu$ A



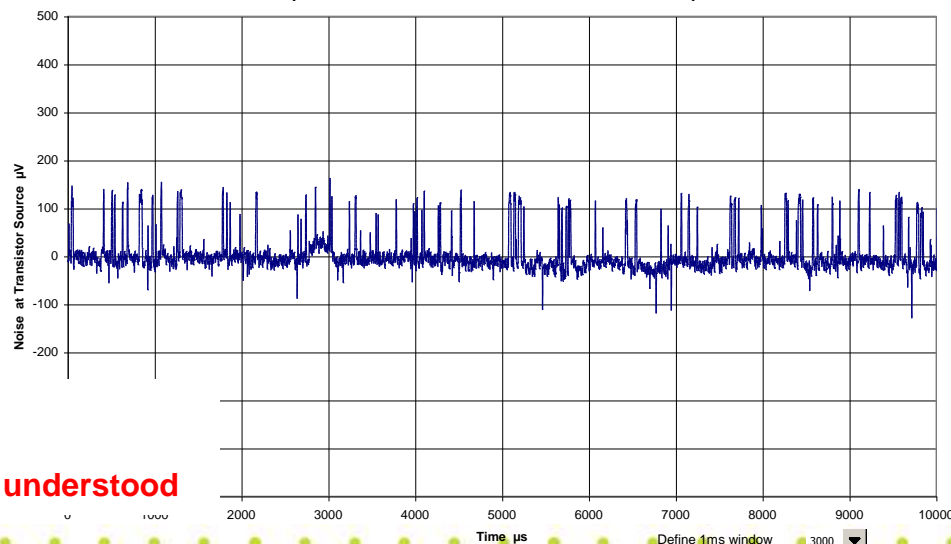
RTS noise plot of CMOS Test Transistor W1-5 at a current of 2 $\mu$ A



RTS noise plot of CMOS Test Transistor W1-5 at a current of 5 $\mu$ A



RTS noise plot of CMOS Test Transistor W1-5 at a current of 10 $\mu$ A



New from e2V – David Burt

Note modest amplitude - ~200  $\mu$ V peak-peak

Wide pixel-to-pixel variation - mechanism is not fully understood

- RT noise is the dominant residual noise source in charge-coupled CMOS pixels. May be triggered by the same mechanism as  $1/f$  noise (tunnelling of charge carriers to *bulk traps* in the oxide) but there's more to it. Maybe the filled trap is critically located near an imperfect source or drain contact, or it may trigger a flow of dark current from a region adjacent to the conducting channel. Some suggestive evidence from studies of RT noise in memory devices (D Burt)
- $1/f$  noise (and possibly RT noise) can in principle be reduced by using a **buried-channel MOSFET** for the source follower. However, producing such devices in the DSM process is a matter of ongoing R&D (e2V and Tower working together). We have seen similar problems with BC transistors from Jazz, but Janesick has been successful, so it isn't fundamental.
- RT noise can be effectively suppressed by the in-pixel CDS logic already envisaged to eliminate reset noise



# Cost estimate

- For a tracking system starting construction ~2020, estimates are pretty speculative
- Assume the 'SLD Vertex' approach, as opposed to the typical astronomy approach of fully tested Grade A devices
- This means a simple **DC-pass acceptance test by vendor**, with full testing by customer (yield was >95% for 8.0x1.6 cm<sup>2</sup> SLD devices)
- Based on *current* Jazz processing costs, we estimate ~\$1k per 8x8 cm<sup>2</sup> thinned device
- 12,700 devices (tracking) plus 17,900 devices (timing) → \$30M total, but device costs will fall with expanding markets
- Add ~10% for mechanics and off-device electronics
- Somewhat more expensive than SiD tracker, but it remains a small fraction of the overall detector cost, and after taking into account the LC running costs, it could be a clear winner



# Possible SPT for LHC

- Same motivation – much reduced material budget. Discovery potential will remain speculative unless such a tracker is built
- Remarkably, expected hit rates at luminosity of HL-LHC (from S McMahon) still permit the architecture with time-integrating tracking layers, where integration time is here a comfortable, low power rolling shutter readout time of  $\sim 1 \mu\text{s}$
- Is radiation hardness OK for tracking layers? It helps that these are already low-resistivity structures, and we aren't pushing to go below  $\sim 30$  cm radius
- A clear challenge is 100% duty factor for timing layers with 25 ns resolution, for which power dissipation implies liquid or evaporative cooling. Possible ways forward:
  - Pre-charge front-end source follower into subthreshold region (14 times lower current for 3 times lower  $g_m$ ) **(but there may be stability issues)**
  - ( $0.13 \mu\text{m}$  or  $0.09 \mu\text{m}$  process and responsivity  $>100 \mu\text{V/e}^-$ ) **(tunnelling currents OK)**
  - Hybrid pixels for these layers
- Track trigger based on timing layers mini-vectors, linked to VXD vectors?
- There is diminished expertise in UK HEP groups for device simulation (Synopsis-TCAD or Silvaco-TCAD). Fortunately, the CEI group at Open U (Andrew Holland) has the capability.
- They have a particular synergy with CMOS pixel expertise at e2V Chelmsford, working with Tower/Jazz. Well-matched to the 'economic impact' aspirations of STFC
- Note also the sCMOS devices and cameras from Fairchild/Andor (UK)/PCO

# Conclusions

- The SPT offers the possibility of high performance tracking over the full polar angle range, with a major reduction in material in all directions, particularly the forward region
- For multi-jet physics (where there's nearly always some activity in the forward region) this looks particularly appealing
- In general, having nearly all the photons convert in the ECAL (or just before it, in timing layers) is desirable
- **These advantages need to be established and quantified by simulations, which are now beginning for the LC applications (ILC and CLIC)**
- The needed pixel technology is currently available, though some development may be needed to make timing layer devices that satisfy the CLIC and LHC requirements
- For LHC, need to check the radiation hardness of such devices
- The LC detector community will probably not have enough resources to sustain all the R&D needed for this, but much is being developed for astronomy and SR applications, not to mention night vision. Goji Etoh, Jim Janesick and others are keen to collaborate, sustained by a recent US Government grant. An inter-disciplinary approach to this R&D looks promising.
- By 2020, 40 Gpixel systems for science will be common. Attitudes in our community are more positive than when we started 30 years ago with pixel-based vertex detectors ...



## SOME EXPERT OPINIONS IN 1980

"Put such a delicate detector in a beam and you will ruin it".

"Will work if you collect holes, not electrons".

"Far too slow to be useful in an experiment".

"It's already been tried; didn't work".

"It will work but only with  $\leq 50\%$  efficiency".

"To succeed, you will have to learn to custom-build your own CCDs: investment millions".

"At room temp it would be easy, but given the need to run cold, the cryogenic problems will be insurmountable".

"May work in a lab, but the tiny signals will be lost in the noise (RF pickup etc) in an accelerator environment".

However, Wrangy Kandiah from AERE, Emilio Gatti and Franco Manfredi from Milano, Veljko Radeka from BNL, Joe Killiany from NRL, Herb Gursky from Harvard Smithsonian were supportive

PPESP found it 'too speculative'; but Erwin Gabathuler, then director of EP Div in CERN, kindly came to our rescue