Supercomputing Systems

Project H1 L2FTT

Detailed Specification

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1 Index

2 Introduction

2.1 Purpose of this document

The purpose of this document is to define all interfaces of components built by SCS. It allows to decouple the work going on at SCS from all other groups during the implementation phase of the project.

The acceptance part defines all criteria / procedures which will be used in order to test and to accept the boards by IPP.

The document will have to be accepted by SCS as well as by IPP and will be referenced in the contracts for all coming work packages.

Documentation about the internal design of the card will be provided in the design description. The latter will be updated during implementation and commissioning of the system in order to deliver a complete documentation at the end of the project.

2.2 Status of this document

The state of this document is draft.

2.3 Open issues / questions

Are marked in RED.

3 HW Interfaces Main Board

3.1 PCB dimensions

6U VME height (233.35 mm) x 220.0 mm depth.

3.2 Backplane Connector VME

3.2.1 Type, Position

DIN 96 pin connector placed according to VME specification. See 3.3.1 .

3.2.2 Pin Assignments

Scott ?

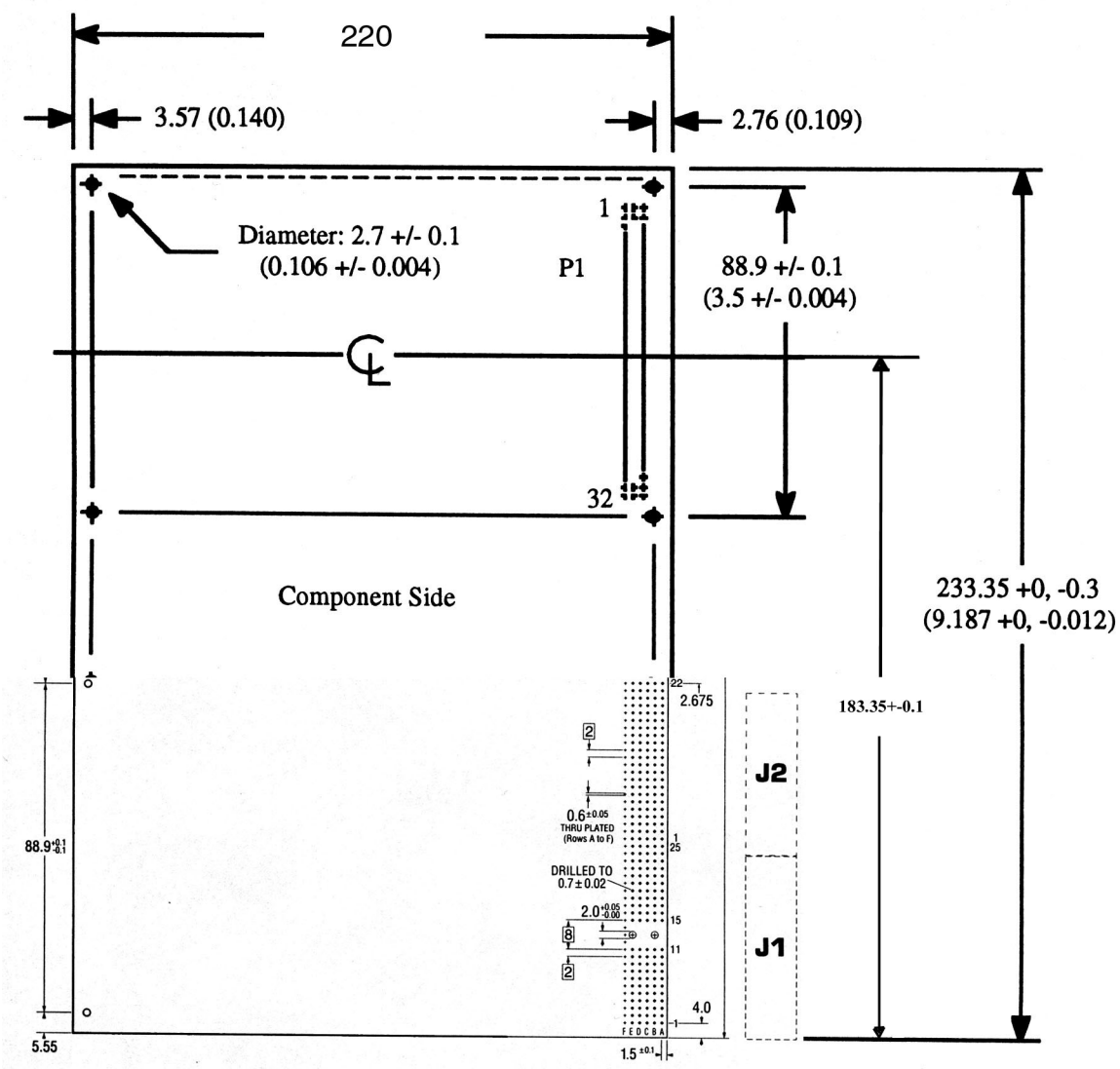
3.2.3 Electrical Properties / Requirements

Scott ?

3.3 Backplane Connector Custom (P2)

3.3.1 Type, Position

Hard metric connector type A with shield and connector type B with shield.
Position according to the 6U CompactPCI standard (lowermost two connectors J1 and J2 only).
The CompactPCI connector has a very long wipe and is compatible with the VME din connector.



3.3.2 Pin Assignments

	a	B	c	D	e
1	Geo1	Geo2	Geo3	Geo4	Geo5
2	5	5	GND	5	5
3	-5	-5	GND	-5	-5
4	GND	GND	GND	GND	GND
5	GND	NC	GND	GND	NC
6	NC	NC	GND	NC	NC
7	NC	NC	GND	NC	NC
8	NC	NC	GND	NC	NC
9	NC	NC	GND	NC	NC
10	NC	NC	GND	NC	NC
11	NC	NC	GND	NC	NC
12	NC	NC	GND	NC	NC
13	NC	NC	GND	NC	NC
14	NC	NC	GND	NC	NC
15	NC	NC	GND	NC	NC
16	NC	NC	GND	NC	NC
17	NC	NC	GND	NC	NC
18	NC	NC	GND	NC	NC
19	NC	NC	GND	NC	NC
20	NC	NC	GND	NC	NC
21	NC	GND	GND	NC	GND
22	3.3	3.3	3.3	3.3	3.3
23	GND	GND	3.3	GND	GND

*

	a	b	c	d	e
24	Spare1	Spare2	1.8	1.8	HClk+
25	1.8	1.8	STC1+	1.8	HClk-
26	STC2+	1.8	STC1-	1.8	1.8
27	STC2-	1.8	1.8	1.8	STC3+
28	1.8	1.8	STC4+	1.8	STC3-
29	Alarm1	1.8	STC4-	1.8	1.8
30	Alarm2	1.8	GND	1.8	Alarm4
31	Alarm3	1.8	GND	GND	GND
32	GND	GND	FastClk+	GND	GND
33	3.3	3.3	FastClk-	3.3	3.3
34	Lugs	identifying	crate as	L1 or	L2
35					
36					
37	3.3	3.3	3.3	3.3	3.3
38	TE0	TE8	3.3	TE16	NC
39	TE1	TE9	3.3	TE17	NC
40	TE2	TE10	3.3	TE18	NC
41	TE3	TE11	GND	TE19	NC
42	TE4	TE12	GND	TE20	NC
43	TE5	TE13	GND	TE21	NC
44	TE6	TE14	GND	TE22	NC
45	TE7	TE15	GND	TE23	NC
46	NC	NC	GND	NC	NC
47	NC	NC *	GND	NC	NC

3.4 Free space backplane / power connector

Between VME connector and the hard metric connectors some space is left free. A custom power connector will be placed there in order to allow the card to be powered in a test environment without the FTT backplane.

* NC: Are any power- / GND signals needed here?

3.5 Piggyback Connectors

3.5.1 Type, Position

A SAMTEC QTE-060-01-L-D-LC will be used. Exact Position will be defined by SCS.

3.5.1.1 Pin Assignments

Pin		Pin		Pin		Pin		
1	PB_DATA0	41	PB_DATA20	81	PB_DATA40			
2	PB_DATA1	42	PB_DATA21	82	PB_DATA41			
3	VCC1.8	43	VCC3.3	83	VCC-5.0			
4	VCC1.8	44	VCC3.3	84	VCC-5.0			
5	PB_DATA2	45	PB_DATA22	85	PB_DATA42			
6	PB_DATA3	46	PB_DATA23	86	PB_DATA43			
7	VCC1.8	47	VCC3.3	87	VCC-5.0			
8	VCC1.8	48	VCC3.3	88	VCC-5.0			
9	PB_DATA4	49	PB_DATA24	89	PB_DATA44			
10	PB_DATA5	50	PB_DATA25	90	PB_DATA45			
11	VCC1.8	51	VCC5.0	91	VCC-5.0			
12	VCC1.8	52	VCC5.0	92	VCC-5.0			
13	PB_DATA6	53	PB_DATA26	93	PB_DATA46			
14	PB_DATA7	54	PB_DATA27	94	PB_DATA47			
15	VCC1.8	55	VCC5.0	95	ID0			
16	VCC1.8	56	VCC5.0	96	ID1			
17	PB_DATA8	57	PB_DATA28	97	PB_CLK1			
18	PB_DATA9	58	PB_DATA29	98	PB_CLK2			
19	VCC1.8	59	VCC5.0	99	ID2			
20	VCC1.8	60	VCC5.0	100	ID3			
21	PB_DATA10	61	PB_DATA30	101	HERACLK			
22	PB_DATA11	62	PB_DATA31	102	GND			
23	VCC1.8	63	VCC5.0	103	TRST			
24	VCC1.8	64	VCC5.0	104	TDO1			
25	PB_DATA12	65	PB_DATA32	105	TDI0			
26	PB_DATA13	66	PB_DATA33	106	TMS			
27	VCC3.3	67	VCC-5.0	107	TCK			
28	VCC3.3	68	VCC-5.0	108	PB_CTRL0			
29	PB_DATA14	69	PB_DATA34	109	PB_CTRL1			
30	PB_DATA15	70	PB_DATA35	110	PB_CTRL2			
31	VCC3.3	71	VCC-5.0	111	PB_CTRL3			
32	VCC3.3	72	VCC-5.0	112	PB_CTRL4			
33	PB_DATA16	73	PB_DATA36	113	PB_CTRL5			
34	PB_DATA17	74	PB_DATA37	114	PB_CTRL6			
35	VCC3.3	75	VCC-5.0	115	PB_CTRL7			
36	VCC3.3	76	VCC-5.0	116	PB_CTRL8			
37	PB_DATA18	77	PB_DATA38	117	PB_CTRL9			
38	PB_DATA19	78	PB_DATA39	118	PB_CTRL10			
39	VCC3.3	79	VCC-5.0	119	PB_CTRL11			
40	VCC3.3	80	VCC-5.0	120	PB_CONNECTED			

3.5.1.2 Electrical Properties / Requirements

Four different supply voltages are carried through this connector:

8 pins for 5.0 Volts
12 pins for 3.3 Volts
12 pins for 1.8 Volts
14 pins for -5.0 Volts

All GND current flows through the shield.

3.6 Power Supply

1.8 V and 3.3 V are provided via backplane connector.

Requirements:

30 W at 3.3 V
14 W at 1.8 V

Core voltages for the DSPs are generated from the 3.3 V supply on the board itself.

Appropriate power sequencing for the DSPs is guaranteed on the board. For all other devices on the board power sequencing is of no importance. (The sequence of 1.8 and 3.3 V power-up does not have any influence on the board. No damage of the board occurs, if one of the two supplies is missing.)

Max ratings (damage levels): the Altera 20ke devices accept a maximum of 2.5 V core and 4.6 V IO. The same applies to the DSPs.

Fuse and over-voltage protection will be implemented if possible.

3.7 Cooling

Cards will be placed in crates with active air circulation, with a maximal inlet temperature of 50° C.

The air is guaranteed to be dry enough such that no moisture problems are to be expected.

3.8 External clock / synchronisation signals

The 'FastClk' running at 10.4 MHz is converted with a LVDS Receiver to LVTTL for synchronization purpose. There are two PLLs for 2x and 5x frequency multiplication (synchronous option). A second LVDS clock from the CompactPCI Connector (HeraClock) will not be used. See Design Description.

4 Additional 'slow' synchronization Signals (STC1…STC4) are received via LVDS from the backplane and made available to both FPGAs on the board (L1Keep etc., according to Service Module).

3.9 Digital output signals ('Trigger Elements')

24 signals on the backplane can be driven by the DataCtrl FPGA. They are buffered e.g. by 74LVT244 driver.

3.10 Test connectors

For DSP debugging purpose there is a emulation connector.

Each FPGA (DataCtrl, DspCtrl) has its own test connector (16 pins + Clock). It's a Mictor Test Connector (view HP: E5346A/E5351A High Density Adaptor Cable Installation Note)

LEDs:
There are 4 LEDs for each FPGA on the main board. 2 green and 2 red ones.

4 HW Specifications Main Board Internal

4.1 Clock / PLL

See Design Description.

4.2 FPGAs

In general there are four FPGAs on the main board: DspCtrl, DataCtrl, VmeCtrl and DpramIf.

DspCtrl is always a EP20K200EFC672-1

DataCtrl can be:
- Fitter / Merger Card: Altera EP20K400EFC672-1X
- Linker Card: Altera EP20K600EFC672-1X

VmeCtrl is an Altera 10k30 (Scott ?)

DpramIf is a MAX7064B-3 or similar. (No external configuration device needed.)

4.2.1 Configuration

There are two JTAG chains from the VME interface, one connected to de devices on the main board, the second one is feeding all FPGAs and EEPROMS on the PiggyBack cards. There will be an additional JTAG plug to connect to the first chain independently for FPGA configuration without the VME IF.

No EEPROMS (EPCx) will be foreseen for configuration (except for VME IF).
There's an additional Driver (74LVT244) to guarantee proper JTAG operation.

4.3 DSPs

There are four floating point DSP TMSC6701GJC16719V running at 166 MHz. They all have their own SRAM for table intensive calculations. Program code will be executed in internal DSP RAM. It's been loaded out of external DPRAM that's written during boot time over the VME bus interface.

4.3.1 SRAM

Two static RAM (SBRAM) CY7C1324-100AC (128k x 18) are provided for each DSP to achieve 32 Bit access. (A total of 8 SRAMs per board)

4.3.2 DPRAM

Two DRAMs CY7C026V-25AC are needed to boot the DSPs (32 Bit access). In main boards without any DSP, it might be used to save messages from the FPGAs that need to be accessed from VME Bus.

4.4 Local Bus

4.4.1 VME Controller

There will be a EPC2 device for VME FPGA configuration. It can be configured over the JTAG interface.

Pin out? -> Scott

Deadline -> Mid November?

4.4.2 CPLD: DpramIf

This interface is needed to convert the asynchronous DPRAM interface to a synchronous one that works together with the VME interface.

4.4.3 I2C: board identification

There is I^2C EEPROM to identify the main board. To identify the piggybacks this bus is no use because one can't locate the cards physically (all are connected in parallel).

5 HW Specification PB Cards

5.1 PCB dimensions

100 mm in height x 150 mm in depth.

5.1.1 Position Piggyback connectors

A SAMTEC QSE-060-04-L-D-LC with 120 contacts will be used for each piggyback board. Pin-out see 3.5.1.1

5.2 Signals to / from PB cards

5.2.1 FPGA data

Input/Input Board:
There are 2x48 Bit of data in parallel coming from the LVDS receivers with a clock frequency of up to 104 MHz.

Input/Output Board:
48 Bit of data in parallel coming from the LVDS receivers with a clock frequency of 104 MHz.
48 Bit of data is transmitted over LVDS out of the FPGA (EP20k60EFC324-1X or EP20k100EFC324-1X).

Additionally there are 48 bi-directional data lines plus 12 control lines down to main board.

5.2.2 Clock

There is a 105 MHz clock oscillator for test purpose. Usually this clock is distributed from the main board over a piggyback connector.

In addition, the clock multiplication as used on the main board (x5 x2) be available on the prototypes for test purposes.

5.2.3 FPGA configuration

All cards are equipped with an EPC2 device in the JTAG chain. The EPC2 devices will be placed in sockets, such that (as a worst case scenario) they can be programmed externally. For configuration during the commissioning phase, a JTAG connector is foreseen on the PB boards. This connector will however have to be removed before the cards can be installed in a fully equipped crate, due to the missing space.

5.2.4 Board identification

As mentioned earlier I2C can't be used for identification. There are 4 pins (16 combinations) to identify each board, read out over DataCtrl, local bus, VmeCtrl on the main board.

5.3 Power

Four different supply voltages may be carried through these connectors:

2 A at 5 Volts
3 A at 3.3 Volts
3 A at 1.8 Volts
3.5 A at -5.0 Volts

See section 3.5.1.2 . Samtec does not provide any numbers on the max. current per pin. We assumed that 250 mA per pin should be no problem.

5.4 LVDS Connectors

5.4.1 Pin Assignments

1	***MP+***
2	*GND*
3	**A0+**
4	**A1+**
5	**A2+**
6	**CLK+**
7	*GND*
8	*GND*
9	**A3+**
10	**A4+**
11	**A5+**
12	**A6+**
13	**A7+**
14	***MP-***
15	**A0-**
16	**A1-**
17	**A2-**
18	**CLK**-
19	GND
20	*GND*
21	**A3-**
22	**A4-**
23	**A5-**
24	**A6-**
25	**A7-**
26	*GND*

MP+/- is an multipurpose signal e.g. for asynchronous serial data transmission/reception or retransmit signalization. In case of an LVDS input channel this is an output otherwise it is an LVDS input .
For LVTTL to LVDS transformation of that signal an National DS90LV019TMX or DS90LV027TMX is used.

5.5 LVDS Cables

Cable type 14526-EZHB-XXX-0QC [1], see 3M Datasheet TS 0891-05 [2] for details.

The electrically equivalent but halogen free (IS23 Standard) version of the cable will be purchased for the final installation.

6 Acceptance Procedures

Acceptance procedures are defined here and will be used

- for the acceptance of the design
- for testing every card before its hand-over from SCS to IPP.

If the acceptance criteria are not met by the design, IPP can request a redesign (several redesigns if needed), according to the procedures defined in the Rahmenvertrag. Additional internal cost will be carried by SCS. External costs (layout, production, new components) will not be covered by SCS.

After acceptance of the design, the series can be produced. The purpose of testing the series is to identify faulty cards and to patch these if possible.

All relevant tests will be carried out at SCS. Testing will be done by SCS staff, in collaboration with IPP as far as wished by IPP. They can be repeated at any other location without impact on the formal acceptance.

6.1 Configuration

6.1.1 VME Controller

The VME controller is configured from the attached EPC2 device. SCS guarantees that configuration is done correctly and that the FPGA is connected to the other devices according to the schematics / design

[1] The halogen-free version of the cable will get a slightly different code.

[2] Warning: some older versions of that data-sheet show an incorrect pinout.

rules provided by IPP. SCS does not take any further responsibility with respect to the VME controller (Local Bus, JTAG, I2C).

6.1.2 DSP controller / data controller

SCS guarantees that these FPGAs can be directly configured using the ALTERA MasterBlaster.

Configuration through the VME Controller can only be tested on the SCS cards after the successful testing of this mechanism on the FEM boards. Functionality is guaranteed by SCS if the JTAG specs are correctly implemented in the VME Controller.

6.1.3 DSPs

One DSP can be operated using the JTAG emulator.

All DSPs can be booted from DPRAM. SCS guarantees proper operation of that mechanism if the VME interface accesses the local bus properly.

6.1.4 Piggyback FPGA

The PB FPGA can be configured from its EPC2, the latter can be loaded from PC.

Configuration using the VME Controller JTAG functionality is guaranteed with the restrictions mentioned in 6.1.2 .

6.2 Operation

6.2.1 Data Transmission LVDS

Reliability of the LVDS link is tested using a loop-back configuration of the LVDS IO cards. At all specified transmission rates, a bit error rate of less then 10E-6 must be achieved when using the local clock oscillator and cables of up to 2 m in length. At up to 52 MHz the same bit error rate must be reached for cables up to 5 m in length.

The bit error rate is measured using the prototype of the LVDS IO board. Specific VHDL code is developed by David Meer together with SCS. The results of the test can be viewed using the test connector on the PB card. A prototype of this PB card should be available before the main boards are produced.

The LVDS IF of the II piggyback boards will only be tested after the main boards have been tested.

6.2.2 Data transmission between FPGAs

Data transmission between PB and DataCtrl will be tested for the SCS cards in a similar procedure as in 6.2.1 . Bit error rates of less then 10E-9 are considered to be acceptable. The same holds for the connection between DataCtrl and DspCtrl.

6.2.3 Data transmission via backplane ('Trigger Elements')

No dedicated measurement setup is used to check the data output via the backplane because the timing is not critical. Functionality and signal-levels are checked for all signals using the oscilloscope.

6.2.4 Receiving synchronization signals from the backplane (HClk, PipeEna,...)

Receiving of these signals can only be tested, when service module and backplane are available and known to work properly.

6.2.5 Operation of the DSP

The DSP which is equipped to work with the emulator can be taken into operation first. SCS guarantees the capability to run the emulator.

All DSPs can be booted from DPRAM if the VME interface is working.

A test program will be delivered by SCS in order to test all relevant HW interfaces. These are (f_{Core} = 166 MHz)

- read / write word-access
    - DPRAM
        - Bootload (f_{Core} / 20)
        - Single access (f_{Core} / 20)
        - DMA (f_{Core} / 20)
    - SRAM (single access, DMA, f_{Core} / 2)
    - DspCtrl (single access, DMA, f_{Core} / 4)[3]
- test all TIN / TOUT / IRQ connections between DSP and DspCtrl

No measurable bit error rates.

[3] Consider that this data rate is below the rate of the LVDS link. It is therefore excluded, that a single DSP can cope with the entire data rate received from one link. It is therefore e.g. not guaranteed, that all data arriving on the L2 decision unit can be processed by a single DSP without additional delay. A similar restriction already arizes from the limitation of the FPGA interconnection, where only 24 lines @ 104 MHz are available.

6.2.6 Local bus

Data transfer between the devices attached to the local bus is possible at 10.4 MHz. The VME IF acts as master on the bus.

If the VME IF is not working at the time of the testing of the cards, the DspCtrl will be used as master, while the VME IF FPGA will be kept in reset for this test.

VISA, 18.12.00:

For IPP: For SCS:

_____ _____

(Dr. A. Schöning) (Dr. D. Müller)