power supply
3v3 ?
2v5 ?
1v8 ?

services
20/50/80 MHz
clock, trigger/reset

out
out
out
out
in

6 x ADC card

LVDS RX

Array driver

Array

cluster logic

trigger logic

ECL TX?

to FLT

single FPGA ?

18 cards from CJC1 only

vme interface ?

backplane J1 = VME, J2 = custom, J? = plus power connections for 2v5, 3v3 etc.

J2 = 160 way = 18 x 8 (4 LVDS pairs) + LVDS clocks etc = tight