FEM internal bus

Address Scheme:

17 16 15	14 13 12 11	10 9 8 7 6 5 4 3 2 1 0
device	unit	internal addresses

Hardware Devices (3bit)

0 0 0	ALL front FPGAs
0 0 1	Front FPGA 1
0 1 0	Front FPGA 2
0 1 1	Front FPGA 3
1 0 0	Front FPGA 4
1 0 1	Front FPGA 5
1 1 0	Back FPGA (I/O unit)
1 1 1	VME IF

Logic Units (4bits)

device	**unit#**	**description**	**address range**
Front FPGA	0 0 0 0	spare	-
	0 0 0 1	Shift Register 1	7 bits
	0 0 1 0	Shift Register 2	7 bits
	0 0 1 1	Shift Register 3	7 bits
	0 1 0 0	Shift Register 4	7 bits
	0 1 0 1	Shift Register 5	7 bits
	0 1 1 0	QT parameter	?
	0 1 1 1	spare	-
	1 0 0 0	FIFO messenger (option)	?
	1 0 0 1	CAM block 1 (option)	9 bits
	1 0 1 0	CAM block 2 (option)	9 bits
	1 0 1 1	CAM block 3 (option)	9 bits
	1 1 0 0	RAM block 1 (option)	10 bits
	1 1 0 1	RAM block 2 (option)	10 bits
	1 1 1 0	RAM block 3 (option)	10 bits
	1 1 1 1	FIFO track segm. output	?

device	**unit#**	**description**	**address range**
Back FPGA	0 0 0 0	spare	-
	0 0 0 1	Validator RAM 1 (200k)	1-11? bits
	0 0 1 0	Validator RAM 2 (200k)	1-11? bits
	0 0 1 1	Validator RAM 3 (200k)	1-11? bits
	0 1 0 0	Validator RAM 4 (200k)	1-11? bits
	0 1 0 1	Validator RAM 5 (200k)	1-11? bits
	0 1 1 0	spare	-
	0 1 1 1	spare	-
	1 0 0 0	FIFO messenger (option)	?
	1 0 0 1	Lookup RAM 1 (100k)	1-11? bits
	1 0 1 0	Lookup RAM 2 (100k)	1-11? bits
	1 0 1 1	Lookup RAM 3 (100k)	1-11? bits
	1 1 0 0	Lookup RAM 4 (100k)	1-11? bits
	1 1 0 1	Lookup RAM 5 (100k)	1-11? bits
	1 1 1 0	FIFO track segm. input	?
	1 1 1 1	FIFO track segm. output	?